WHAT IS CLAIMED IS:

1. A Ternary content addressable memory (TCAM) comprising:

an array of TCAM cells arranged in a plurality of rows and a plurality of columns ;

a plurality of match lines, one match line for each row of CAM cells and operatively coupled to a plurality of output transistors for the TCAM cells in the row;

a plurality of dummy lines, one dummy line for each row of TCAM cells and operatively coupled to a plurality of dummy transistors for the TCAM cells in the row;

a plurality of match data bit lines and their complementary, one pair of match data bit line and their complementary for each column of TCAM cells to provide the match data and its complementary to compare with the content stored in each cell of that column;

a column of dummy TCAM cells connected to match line and dummy line in every row correspondingly ;

a pair of dummy match data bit line and its complementary for the column of dummy TCAM cells to provide dummy match data and its complementary to compare with the content stored in each cell of that column;

a column of sense amplifier connected to the match line and dummy line in each row correspondingly ; and

A column of current source connected to match line and dummy line in each row.

2. A Ternary content addressable memory (TCAM) of claim 1, wherein A ternary content addressable memory (TCAM) cell comprising:

a memory cell operable to store a data bit value;

a secondary cell operable to store a control bit value; and

a comparison circuit coupled to the memory cell and the secondary cell and configured to detect the data bit value stored in the memory cell and the control bit value stored in the secondary cell, the comparison circuit including

a pair of output transistors coupled to a match line and configured to provide a drive for the match line based on the detected data bit value and the detected control bit value, and

a pair of dummy transistors coupled to a dummy line to provide a drive for the dummy line based on the detected control bit value , wherein the match line and dummy line are used to detect an output value provided by the CAM cell.

3. A Ternary content addressable memory (TCAM) of claim 1, wherein a dummy ternary content addressable memory (DTCAM) cell comprising:

a memory cell operable to store a data bit value;

a secondary cell operable to store a control bit value; and

a comparison circuit coupled to the memory cell and the secondary cell and configured to detect the data bit value stored in the memory cell and the control bit value stored in the secondary cell, the comparison circuit including

a pair of output transistors coupled to a match line and configured to provide a drive for the match line based on the detected data bit value and the detected control bit value, and

a pair of dummy transistors coupled to a dummy line and configured to provide a drive for the dummy line based on the detected inverted data bit value and the detected control bit value.

4. The DTCAM cell of claim 3, wherein the dummy transistors have smaller dimension and less driving ability than the output transistors, are located in close proximity to the output transistors, and are turned ON during sensing operation to enable the comparison of the corresponding row.
5. The DTCAM cell of claim 3, wherein the dummy transistors are turned OFF and the output transistors are turned ON during sensing operation to disable the comparison of the corresponding row.

6. A Ternary content addressable memory (TCAM) of claim 1, wherein a sense amplifier connected to match line and dummy line of each row comprising:
two inverters connected to each other in a way of positive feedback;
a P transistor serially connected to both two inverter and Vdd ;
two N transistors serially connected to each inverter and Ground.

7. A Ternary content addressable memory (TCAM) of claim 1; wherein two P transistor connected to match line and dummy line of each row and Vdd to provide current sources from Vdd to match line and dummy line.

8. A Ternary content addressable memory (TCAM) of claim 1; wherein two N transistor connected to match line and dummy line of each row and Ground to provide discharge channel from match line and dummy line to Ground .

9. A method of detecting a match or miss state of the comparison result, comprising the following sequential steps:

set the current source P transistors of claim 7 to OFF state and there is no current flowing from Vdd to match line and dummy line,

set the P transistors of claim 6 to OFF state to disable the sense amplifier;

set the N transistors of claim 6 to ON state to build a conducting path from match line and dummy line to Ground and discharge dummy line and match line to ground;

build a conducting path from match line and dummy line to Ground and make the potential of dummy line and match line equal to the potential of ground through turning on the N transistors of claim 8 ;

After the voltage potential of both match line and dummy line are equal to ground voltage potential, turn off the N transistors of claim 6 and 8;

send the match data and their complementary into the TCAM cells through the match bit (mbl) line and their complementary (mblb) of claim 1;

send the dummy match data and its complementary into the column of dummy TCAM cells through dummy match data bit line and its complementary;

enable the current source P transistors of claim 7 and build a conducting path from Vdd to match line and dummy line, and pull the potential of match line and dummy line to the level less than half Vdd;

disable the current source P transistors of claim 7 and shut off the conducting path from Vdd to match line and dummy line; and

turn on the P transistor of claim 6 and enable the sense amplifier to sense the voltage difference between each pair of match line and dummy line to determine the match or mismatch state; wherein finish one comparison cycle.